Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1-7. (Cancelled)

8. (Previously Presented) A transistor comprising:

a semiconductor substrate, the substrate being substantially free of silicon and selected from the group consisting of indium antimonide, lead telluride, indium arsenide, indium phosphide, , and gallium antimonide; ~~and~~

a gate dielectric layer formed over a portion of the substrate, wherein the gate dielectric layer comprises a ~~material~~ metal oxide having a dielectric constant greater than 7.8, wherein a portion of the gate dielectric layer has a thickness that is large enough to reduce gate leakage current, and wherein the material comprises a compound having a free energy of formation that is lower than a free energy of formation of a compound that is formed between the material and the semiconductor substrate; and

a gate electrode defined over a portion of the gate dielectric layer such that the gate dielectric layer has a cross-sectional area substantially similar to a cross-sectional area of the gate electrode.

9. (Canceled)

10. (Previously Presented) The transistor of claim 8, further comprising:

a source region and a drain region proximate the gate electrode, the source and drain regions defined by introduced ions.

11. (Original) The transistor of claim 10, further comprising:

an interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region

12. (Original) The transistor of claim 11, wherein the interlevel dielectric defines first, second, and third openings in the interlayer dielectric layer over at least part of the gate electrode, the source region, and the drain region.

13. (Original) The transistor of claim 12, further comprising:

a metal within the first, second, and third openings in contact with the gate electrode, source region, and the drain region.

14. (Original) The transistor of claim 8, wherein the substrate comprises a material having a carrier mobility greater than a carrier mobility of silicon.

15. (Canceled)

16. (Previously Presented) The transistor of claim 8, wherein the substrate has a bandgap narrower than a bandgap of silicon.

17. (Currently Amended) The transistor of claim 16, wherein the gate dielectric comprises at least one of aluminum oxide, hafnium oxide, zirconium silicon oxide, strontium titanium oxide, tantalum oxide, barium titanium oxide, zirconium oxide, yttrium oxide, and barium strontium titanium oxide~~, and silicon nitride~~.

18. (Previously Presented) The transistor of claim 8, wherein the gate electrode comprises at least one of titanium nitride, tantalum nitride, titanium, tantalum, nickel, platinum, polygermanium, and polysilicon.

19. (Currently Amended) A device comprising:

a semiconductor substrate, the substrate being substantially free of silicon and selected from the group consisting of indium antimonide, lead telluride, indium arsenide, indium phosphide, and gallium antimonide;

a well formed in a portion of the substrate, the well having a first type of dopant;

a gate dielectric layer formed over a portion of the well, wherein the gate dielectric layer comprises a ~~material~~ metal-oxide having a dielectric constant greater than 7.8, wherein a portion of the gate dielectric layer has a thickness that is large enough to reduce gate leakage current, and

wherein the material comprises a compound having a free energy of formation that is lower than a free energy of formation of a compound that is formed between the material and the semiconductor substrate;

a gate electrode defined over a portion of the gate dielectric layer such that the gate dielectric layer has a cross-sectional area substantially similar to a cross-sectional area of the gate electrode; and

a source region and a drain region defined proximate the gate electrode in the well, the source and drain regions being defined by a second type of dopant.

20. (Original) The device of claim 19, wherein the first dopant is n-type and the second dopant is p-type.

21. (Original) The device of claim 19, wherein the first dopant is p-type and the second dopant is n-type.